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(51) **International patent classification**[6]: **HO1L 21/66, G01R 31/3185**	**A1**	**(11) International publication number: WO 99/17353** **(43) International publication date:** April 8, 1999 (04/08/99)

(21) International reference: PCT/DE98/02566

(22) International application date: Sept. 1, 1998 (09/01/98)

(30) Priority dates:
197 42 946.7 September 29, 1997 (09/29/97) DE

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(81) Designated countries: CN, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: MULTIPLEXED TEST CIRCUIT ON A SEMICONDUCTOR CHIP

(illustration)

(57) Abstract

The invention relates to a test circuit on a semiconductor chip, comprising test components on metering runs, which are connected by conductor paths with the contact areas. In order to determine the features of the components, test signals or measurement signals are sent to the contact areas, then removed therefrom. The outputs of the selection logical circuit activate metering runs with at least one test component by run, thereby enabling the measurement signals of various test components to be recorded on one contact area. One test circuit according to the invention enables the number of contact areas required to be substantially reduced.

Description

MULTIPLEXED TEST CIRCUIT ON A SEMICONDUCTOR CHIP

The invention relates to a test circuit on a semiconductor chip with test components in measured sections, which are connected via conductor paths with contact surfaces for sending and removing test signals or measurement signals, for determining characteristic values of the test components.

The measurement of technological parameters or characteristic values on semiconductor chips, such as, for example, the current yield of NMOS/PMOS transistors, high-value or low-value poly resistors on the wafer level, is of great significance for error analysis in analog and mixed-signal circuits. Traditionally, this measurement is carried out via a plurality of contact surfaces, so-called pads, which are usually arranged, together with other contact surfaces, in a pad frame outside the area of the circuit. Through gauging tips and the like, the contact surfaces are accessed by external measuring systems, which in turn are connected via conductor paths to the measured sections containing the components to be tested.

With the progressive reduction in circuit size on chips, the size of the chips is increasingly being determined by the contact surfaces. If there is the threat of the chip surface, due to the contact surfaces for determining the technological parameters, becoming larger than is absolutely required for the actual function of the chip, this surface problem can be addressed only by omitting contact surfaces. Experience shows, however, that in subsequent error analysis, this omission results in much more work, because the technological parameters needed for the analysis were not available in the required quality and quantity.

The invention is based on the task of providing a test circuit of the type mentioned at the start, in which the number of measured sections is increased and yet little chip surface is used.

The solution of this task according to the invention lies in that there is a signal-controlled selection logic circuit that exhibits at least one control signal input connected with a contact surface, that the selection logic circuit outputs are connected to control inputs of measured sections, each exhibiting a test component, and that all measured sections are connected to only one contact surface on the output side.

A central idea of the invention lies in that, from the plurality of measured sections, one measured section each is individually selected, using a type of addressing. The number of contact surfaces and control lines required for the selection logic depends on the number of measured sections and the type of control signals containing the addressing, as well as the transmission method. In a sequential transmission, all control signals for a practically unlimited number of measured sections can be transmitted on a single line. In parallel transmission, the minimum number of contact surfaces depends on the address coding selected and on the number of measured sections. For example, using binary code, control signals for 2^n measured sections can be transmitted over n lines.

Because each measured value can be chronologically classified in a unique manner, through the deliberate choice of one measured section, all measured values can be sent on only one line to one single contact surface and can be accessed there.

In this way, there is definitely less space requirement, since at least one contact surface is to be provided for the traditional test circuits for each component. Furthermore, even areas that are far removed from the contact surfaces can be used, at little

cost, for the arrangement of test components, since the number of conductor paths connected to them is reduced to the same extent as the number of contact surfaces.

It is particularly favourable to design the measured sections in such a way that, on the output side, they all yield the same measured variable, e.g., current or voltage, to the contact surfaces. Thus, for example, the current yield of various transistor types and specific resistances of various resistor types can each be directly determined through current measurements. In this way, only one current or voltage source need be accessed, and the sending of the measured value can be done without much outlay of lines.

It is advantageous for all outputs of all measured sections to be connected to the contact surface that is connected to a control signal input of the selection logic circuit. As a result of this double usage of a contact surface, the number of total contact surfaces needed is further reduced. Such utilization of a contact surface and the conductor path connected thereto for bi-directional communication requires an exact specification of when the contact surface can be supplied with signals and when the measured sections can give off output signals. Otherwise, this can result in incorrect measurements and erroneous interpretations or in the selection logic circuit ignoring the control signals.

Furthermore, it is advantageous for the selection logic circuit to exhibit a clock-pulse generator and a control mechanism, for the control mechanism to be connected on the input side with an output of the clock-pulse generator, and for the control mechanism to be connected on the output side with the signal inputs of the measured sections. With the clock-pulse generator, a chronological basis is available, through which the activation duration of the measured sections can be defined. Thus, it is

possible, for example, to design the test circuit such that, after impinging on the contact surface connected to the control signal input of the selection logic circuit, a predetermined activation sequence of the measured sections is triggered with a defined signal. For example, through a simple change in level on the control signal input, it is possible to trigger a sequence in which individual measured sections are each activated after a specific number of cycles, in order to be deactivated again after a likewise specific number of cycles. In this way, it can be ensured that, in accordance with the control signal that triggers the measurement sequence, only one measured section is always activated each time, and activation times and intervals between the individual activations that can be set individually are maintained for the measured sections.

A preferred embodiment of the invention is characterized in that the selection logic circuit exhibits a shift register with several D flip-flops whose clock inputs are switched in parallel, that the input of a first D flip-flop is switched at the level of logical "0", that the inputs of the other D flip-flops are each connected with the output of a D flip-flop connected to them, and that the outputs of the D flip-flops are connected with the signal inputs of the measured sections. A test circuit designed in such a manner can, with extremely low outlay in circuits, execute a defined activation and de-activation sequence of the measured sections. Even in this instance, a simple change in level on a control input of the test circuit would already be necessary in order to trigger the predetermined activation and de-activation sequence. The level signal can, for example, be sent to the SET input of the first D flip-flop and to the RESET inputs of the other D flip-flops. After the clock inputs of all D flip-flops are switched in parallel, an activation signal, whose duration is defined by the frequency and impulse/interval ratio of the cycle, is sent individually to the signal inputs of the measured sections one after the other in the cycle created on the

clock inputs of the D flip-flops. If the selection logic circuit already exhibits a clock-pulse generator that is permanently in operation, a single contact surface would suffice for the test circuit. Through this, the control signal for triggering the activation/de-activation sequence, e.g., a LOW-level signal, could be sent, making possible a subsequent consecutive measurement of the test components in the measured sections.

A preferred embodiment of the invention is characterized by the fact that the selection logic circuit exhibits a decoder for decoding control signals that describe the addresses of measured sections. Measured sections can consequently be deliberately activated. No specified activation and deactivation sequences of the measured sections therefore need to pass through if only one measured section is supposed to be activated. In this case, the coding of the control signals may take place in the most varied manner. For example, it is possible to define control signal telegrams through change of level sequences on only one control line. A further possibility lies in addressing a binary register of the measured section addresses via control lines, whose number corresponds with the number of the measured sections. For 2^n measured sections, only n control lines are therefore necessary.

A further preferred embodiment of the invention is characterized in that the selection logic circuit is connected on the input side to a data bus for transferring the addresses of measured sections, and that at least one conductor of the data bus is connected to a contact surface. In this variation as well, a specific selection of individual measured sections is possible. Since there is a plurality of standardized data buses for the most varied purposes, a suitable and proven data bus can be selected therefrom.

Another embodiment of the invention to be preferred is distinguished in that one transistor each is available to connect

the measured sections, the control input of the transistor being connected in each case with an output of the selection logic circuit. With little outlay involved in the circuit technology, transistors can handle the relay function, and connect measured sections when a signal of the selection logic circuit is sent to its control input. The design of measured sections has a particularly simple shape when, for instance, current yields of transistors are supposed to be determined. In this case, it is sufficient for the measured section to exhibit, as the sole component, the transistor to be tested. The control input of the transistor to be tested is connected to an output of the selection logic circuit and the transistor current can be measured, depending on the voltage present on the transistor, through a contact surface connected via a conductor path to the transistor. To determine resistances, the source and drain of the transistor can be switched in series with the resistance. In a corresponding signal on the control input of the transistor, the area between the source and drain becomes conductive, and a current that depends on the resistance to be determined, applied voltage, and characteristic curve, can be measured.

An embodiment of the invention will be described more precisely in the following, with the help of a drawing. To illustrate:

Fig. 1 — the schematic representation of a test circuit with clock-pulse generator, shift register with several D flip-flops, and several measured sections,

Fig. 2 — the schematic representation of the chronological course of the RESET voltage, the clock voltage, and the measured current, as possible with the test circuit schematically shown in Fig. 1.

The figure illustrates an integrated test circuit on a semiconductor wafer, on which there is a plurality of integrated switching circuits, not illustrated. In the example illustrated, the test circuit contains four measured sections 7, 8, 9, 10, which serve to determine technology parameters of semiconductor components in the measured sections through a current measurement. They are therefore connected to a current supply V on the input side. Furthermore, they each exhibit a control input 13, with which the measured section is activated or deactivated. In the simplest case, it is a transistor 16 as a circuit element, which is connected to the measured section. All measured sections 7, 8, 9, 10 of a common line 14 lie on the output side, which leads to a first contact surface 12 to tap the current flowing in a measured section 7, 8, 9, 10, through an external measuring device.

The contact surface 12 is furthermore connected to the input of a sequential selection logic circuit, which consists here of one clock-pulse generator 1, as well as a shift register 15 impinged on the input side by the clock-pulse generator 1, the shift register exhibiting here four D flip-flops 2, 3, 4, 5 connected in series. The setting input SET of the lowest order flip flop 2 is connected to a second contact surface 11 via an inverter 6, which are furthermore connected to the reset inputs R of all remaining flip-flops 3 to 5. The second contact surface 11 serves to execute, from without, a signal to set or reset the individual flip-flops 2, 3, 4, 5.

The measured sections 7, 8, 9, 10 are basically found in the closed state, i.e., no signal is applied to the control input 13 to connect the measured section through. As a result, no output signal of the individual measured sections 7 to 10 is applied even on the line 14.

By feeding control signals via the contact surface 12 to the selection logic circuit, one of the measured sections 7 to 10 is selected by the selection logic circuit, in which the control input 13 concerned is impinged on, as a result of which the appropriate circuit element opens. During the duration of the control, a current flows in the measured section from the current supply V to line 14, which marks the testing component in the measured section. In the controlled circuit element of the measured section, it may be a transistor, which itself represents the component to be tested, as an example of the first measured section 7 illustrates. Another example may exist in that a resistance 17 to be tested lies in the controlled section of a transistor 18 serving as pure circuit element, as shown in the example of the third measured section.

The selection logic circuit via the contact surface 12 is controlled in the present example in such a way that a clock signal U_t (see Figure 2) is sent to the clock-pulse generator 1 on the input CLK. The output signal of the clock-pulse generator 1 causes a logical "1" signal to be pushed through all register points of the shift register 15 (i.e., through the flip-flops 2 to 5). In this manner, a logical 1-signal is present on the output of each consecutive flip-flop 2 to 5, which is correspondingly cycled one after the other to the control inputs 13 of the measured sections 7 to 10.

The clock signal consequently has the function of addressing the individual register points and the measured sections.

The function of the test circuit will be described in detail in the following, using Figures 1 and 2. For initialization, a reset signal RESET, which, in accordance with Figure 2, increases its level from the value 1 to the value h, is entered at time t_1 through the contact surface 11. As a result, the signal on the output Q of the first flip flop 2 takes the logical value "1",

while the outputs Q of all other flip-flops 3, 4, 5 take the logical value "0". The measured section 7 belonging to the first flip-flop 2 is controlled as a result, while the remaining measured sections 8, 9, 10 are blocked. A current consequently flows in the measured section 7, which is measurable on the contact surface 12, and which is unambiguously allocatable to this measured section.

At time t_2, all flip-flops 2, 3, 4, 5 are impinged on by the clock-pulse generator 1 with a timing signal, which lasts until time t_3. Through the connection of an output Q and an input D from two flip-flops following each other, the logical value "1" of the particular flip-flop is pushed into the next flip-flop during timing signal U_t, so that, in accordance with Figure 2, after resetting the first flip-flop 2 at the time t_2 between the time t3 and t4, the logical value "1" is applied to output Q of the second flip-flop 3. The second measured section 8 is electrically connected as a result, while all other measured sections are blocked. The current I_m flowing through the second measured section 8 can thus be measured on the contact surface 12.

In the same manner, the value logical "1" is pushed through the third and fourth flip-flop 4, 5, so that, corresponding to the period of the timing signal U_t, the third and fourth measured distance 9, 10 is electrically connected one after the other between the times t_6 to t_7 or t_8 to t_9.

Patent Claims

1. Test circuit on a semiconductor chip with test components in measured sections (7, 8, 9, 10), which are connected via conductor paths with contact surfaces for sending and removing test signals or measurement signals, for determining characteristic values of the test components,
wherein
there is a signal-controlled selection logic circuit that exhibits at least one control signal input connected with a contact surface,
the selection logic circuit outputs are connected to signal inputs of measured sections (7, 8, 9, 10), each exhibiting a test component,
and all measured sections (7, 8, 9, 10) are connected to only one contact surface on the output side.

2. Test circuit according to Claim 1,
wherein
all outputs of all measured sections (7, 8, 9, 10) are connected to the contact surface that is connected to a control signal input of the selection logic circuit.

3. Test circuit according to Claim 1 or 2,
wherein
the selection logic circuit exhibits a clock-pulse generator (1) and a control mechanism,
the control mechanism is connected on the input side with an output of the clock-pulse generator, and
the control mechanism is connected on the output side with the signal inputs of the measured sections (7, 8, 9, 10).

4. Test circuit according to Claims 1 to 3,
wherein

the selection logic circuit exhibits a shift register with several D flip-flops (2, 3, 4, 5) whose clock inputs are switched in parallel,

the input of a first D flip-flop (2) is switched at the level LOW,

the inputs of the other D flip-flops (3, 4, 5) are each connected with the output of a D flip-flop connected to them (2, 3, 4), and the outputs of the D flip-flops (2, 3, 4, 5) are connected with the signal inputs of the measured sections.

5. Test circuit according to Claims 1 to 3,
wherein
the selection logic circuit exhibits a decoder for decoding control signals that describe the addresses of measured sections.

6. Test circuit according to Claim 5,
wherein
the selection logic circuit is connected on the input side to a data bus for transferring the addresses of measured sections (7, 8, 9, 10), and
at least one conductor of the data bus is connected to a contact surface.

7. Test circuit according to any one of Claims 1 to 6,
wherein
a control signal input of the selection logic circuit is a reset input.

8. Test circuit according to any one of Claims 1 to 7,
wherein
one transistor each is available to connect the measured sections (7, 8, 9, 10), the control input of the transistor being connected in each case with an output of the selection logic circuit.